WAVEGUIDE STRESS ENGINEERING AND COMPATIBLE PASSIVATION IN PLANAR LIGHTWAVE CIRCUITS

Field of the Invention

[0001] The present invention relates to protective passivation layers for planar lightwave circuits. More particularly, the present invention relates to passivation techniques which preserve the stress engineered environment of underlying optical waveguide layers.

Background of the Invention

[0002] Fiber optic communication links have been conventionally employed in long-haul, point-to-point networks with controlled environments at all interface points. Such highly controlled, "central office" surroundings usually offer relatively benign operating environments (temperature, humidity, mechanical) for components. Consequently, highly functional components could be developed and installed without considering the impact of other, more extreme environments.

[0003] Recent technological advances, coupled with increasing bandwidth demand, are rapidly expanding the use of fiber optic components beyond the "central office" and into potentially harsher environments. For example, dense wavelength division multiplexing (DWDM) enables the transmission of multiple, independent wavelength streams across a single fiber. Predictably, this capability has resulted in the requirement to add or drop these optical channels along the previously untapped long lengths of fiber (and outside of the central office environment) to provide access to the individual wavelength streams. Optical add/drop multiplexers (OADMs) are employed for this function, enabled by arrayed waveguide grating (AWG) components for filtering and forwarding individual wavelengths.

[0004] In addition to these technological advances, simple market forces are pushing fiber networks beyond central offices and into the diverse terrain of "metro" markets. This ever-increasing need for bandwidth which only fiber can deliver is resulting in the

widespread deployment of fiber networks, and their associated components, into the harsher, less environmentally controlled conditions present in the metro market.

[0005] The demands placed on component designers now reach far beyond optical performance, and into the realms of thermal, humidity and mechanical insulation. Certain qualification standards (e.g., Telcordia) exist for reliability of optical components, and many customers require qualification under these standards. AWGs however are thin, fragile chips with narrow waveguides produced using planar lightwave circuit (PLC) processing techniques. The various processing tolerances required to meet the requisite optical specifications are already very tight, and in fact get tighter as the need to process more and closer channels increases.

[0006] One particular concern for PLC waveguides, including those in AWGs, is their sensitivity to stress imbalances, and the impact of stress imbalances on optical performance. These stresses can be induced by the environmental conditions discussed above, and by the fabrication process itself. Stress-induced birefringence in waveguides leads to unacceptably high polarization dependent loss (PDL) for communication systems.

[0007] Waveguides are typically fabricated by forming (e.g., etching) waveguide core patterns over a substrate and undercladding. A doped glass overcladding (e.g., boro-phosphate silicate glass or BPSG) is then formed over the cores, to complete the waveguide formation. Because the materials used for these layers are different, with differing properties (e.g., differing coefficients of thermal expansion (CTEs)), intra- and inter-layer stresses exist and will result in high levels of waveguide PDL.

[0008] Techniques have been disclosed to address these problems, such as stress release grooves (SRGs) (see, e.g., Nadler et al, "Polarization Insensitive, Low-Loss, Low-Crosstalk Wavelength Multiplexer Modules," IEEE Journal of Selected Topics in Quantum Electronics, Vol. 5, No. 5, September/October 1999) and tailoring of the overcladding (see, e.g., Kilian et al, "Birefringence Free Planar Optical Waveguide Made by Flame Hydrolysis Deposition (FHD) Through Tailoring of the Overcladding," IEEE Journal of Lightwave Technology, Vol. 18, No. 2, February 2000; and "Simple Method

of Fabricating Polarisation-Insensitive and Very Low Crosstalk AWG Grating Devices," Electronics Letters, Vol. 34, No. 1, January 8, 1998). Such techniques are broadly referred to herein as stress management or stress engineering, which in effect "balance" the stress affecting the waveguides. The term "balance" is known to those in the art and used broadly herein to connote any type of active stress management which provides the requisite, advantageous minimization of birefringence. Multiple stress balancing techniques are disclosed herein.

[0009] Even assuming that such techniques are employed to manage stress, they are still susceptible to the adverse environmental conditions, discussed above. However, any techniques used to protect the circuit from these environmental conditions must also be compatible, and not interfere with, any stress management techniques employed. Modified annealing techniques for the overcladding have been proposed, but have not produced satisfactory protection. Hermetic packaging of the circuits can also provide protection, but such techniques can be expensive, and subject to long-term failures. To decrease reliance on packaging, what is required are advanced techniques to protect planar lightwave circuits from adverse environmental conditions, while maintaining their stress engineered properties at the chip level.

Summary of the Invention

[0010] These requirements are met, and further advantages are provided, by the present invention which in one aspect is a planar lightwave circuit, along with techniques for its formation and use. The planar lightwave circuit includes at least one optical waveguide core, and at least one feature proximate the core having at least one stress-engineered property to balance stress affecting the core. A protective passivation layer is formed over the core and the feature. The passivation layer is formed to be substantially non-interfering with the balanced stress affecting the core provided by the feature.

[0011] The passivation layer has the requisite passivation properties (i.e., protection against environmental conditions against which the devices will be tested), and is compatible with the stress management used in lower circuit layers.

[0012] The stress balancing feature may be an overcladding layer formed over the core, doped to balance stress affecting the core. The overcladding is doped to have a coefficient of thermal expansion approximately matched to that of an underlying substrate to thereby symmetrically distribute stress in an undercladding between the overcladding and the substrate, and therefore away from the core. The protective passivation layer is formed to have a coefficient of thermal expansion approximately matched to that of the overcladding such that it is substantially non-interfering with the balanced stress affecting the core provided by the overcladding. In one exemplary embodiment, the passivation layer is formed from silicon nitride.

[0013] Another optional stress balancing feature is a stress release groove formed through the overcladding between two cores, which releases and therefore balances stress affecting the two cores. A second overcladding may be formed along walls and a floor of the stress release groove to partially but not completely fill the groove to preserve its stress releasing property, but sufficient to support a generally planar portion of the passivation layer over the groove.

[0014] Yet another optional stress balancing feature of the circuit may involve overetched portions of the undercladding, respectively adjacent to opposing lower edges of each core, terminating at a point lower than the cores, to further effect a removal of the stress away from the cores. This lower termination point may correspond with the bottom of the stress release groove to thereby provide an identifiable etch transition point for the stress release groove.

[0015] Regardless of the particular selection of stress balancing features, the passivation layer is designed to be non-interfering with their stress balancing properties, while providing all of the benefits of passivation, including its barrier to vapor, chemicals, etc. This barrier protection is becoming increasingly important as optical components are subjected to more adverse environments, and their related reliability standards and testing.

Brief Description of the Drawings

[0016] The subject matter which is regarded as the invention is particularly pointed out and distinctly claimed in the concluding portion of the specification. The invention, however, both as to organization and method of practice, together with further objects and advantages thereof, may be best understood by reference to the following detailed description of the preferred embodiment(s) and the accompanying drawings in which:

[0017] FIG. 1A is a top plan view of a typical planar lightwave circuit (PLC) with an arrayed waveguide grating (AWG) having closely spaced waveguides in several sections thereof;

[0018] FIG. 1B is a partial cross-sectional view of a typical wafer section showing the cladding layers around cores of several waveguides;

[0019] FIGS. 2A-D depict in cross-section the processing steps used to arrive at certain waveguide configurations in accordance with the present invention;

[0020] FIG. 3 depicts in cross-section a first waveguide configuration of the present invention including a passivation layer;

[0021] FIGS. 4A-B depict in cross-section a second waveguide configuration of the present invention including a passivation layer combined with stress release grooves between the waveguide cores;

[0022] FIGS. 5A-B depict in cross-section a third waveguide configuration of the present invention including buffer and passivation layers, also in combination with stress release grooves between the waveguide cores; and

[0023] FIGS. 6A-B depict in cross-section a fourth waveguide configuration of the present invention, wherein a waveguide core overetch is used as an etch transition point for stress release groove (SRG) etching.

Best Mode For Carrying Out the Invention

[0024] With reference to FIG. 1A, an exemplary planar lightwave circuit (PLC) 10 is shown in the form of an arrayed waveguide grating (AWG) formed over a substrate 20 (e.g., silicon). As known to those in the art, an AWG uses an array of closely spaced waveguides 22 having carefully controlled, differing path lengths which cause constructive phase interference patterns on the respective optical signals transmitted into and out of the device. This technique is useful for multiplexing or demultiplexing optical signals passed between the array input/focusing region 24/25 to the array output/focusing region 26/27. The tight spatial and thermal tolerances necessary for proper operation of array 20, as discussed above, lead to the requirements for effective packaging and sealing for use in adverse environmental conditions. Moreover, as discussed above, waveguides 22 are highly susceptible to stresses, thus imposing the additional requirement of stress engineering during their fabrication.

[0025] FIG. 1B depicts in partial cross-section a typical wafer-based "silica-on-silicon" waveguide configuration, used for waveguides 22 of FIG. 1A. A buffer layer 32 (e.g., a thermal oxide or SiO_2) is formed (e.g., grown or deposited) over a silicon substrate 30. Though various deposition / formation techniques are disclosed herein, those skilled in the art will recognize that any number of known techniques can be used without departing from the principles of the present invention.

[0026] Buffer 32 serves as the "undercladding" for the waveguide cores 34_1 ... 34_3, which are formed from a doped silica glass layer (e.g., doped with phosphorous, germanium, nitride, or any other dopant(s) which appropriately modify the refractive index upward - phosphate silicate glass (PSG) being one example). This layer is etched using, e.g., photolithographic mask and reactive ion etching (RIE) techniques. The term "core" is used broadly herein to connote any type of structure within which light is guided. An "overcladding" layer formed from a doped silicate glass layer 36 (e.g., doped with boron, fluorine, phosphorous, germanium, nitride, or any dopant(s) which appropriately modify the refractive index downward - boro-phosphate silicate glass

(BPSG) being on example) is then deposited over the cores to complete their waveguide configuration.

[0027] As discussed above, techniques are available to ensure that stress imbalances in and around the waveguides do not adversely impact optical performance. These techniques include doping the overcladding, half-lambda compensation plates, and stress release grooves between the waveguides. However, the instant inventors have discovered that the adverse environmental conditions (discussed above) negatively impact these known stress engineering techniques. For example, stress engineering by doping the overcladding reduces the moisture resistance of this layer, and can eventually adversely affect the optical properties of the layer. Any sealing techniques must therefore not only perform their designated task of preventing the flow of moisture, etc.; they must also maintain, and not interfere with, the stress engineered environment of the lower layers.

[0028] In accordance with the present invention, a passivation layer is employed to seal the entire waveguide structure. In one embodiment, silicon nitride is used, but other materials are possible. This passivation layer can be used in combination with certain stress engineering techniques employed in the lower layers. As discussed below, the composition of this layer, and its deposition process, are specially tailored to avoid interfering with the stress balancing in the lower layers. The present invention also extends to certain improvements to the stress engineering techniques themselves.

[0029] FIGS. 2A-2D depict in partial cross-sectional view certain exemplary processing steps used to realize a first embodiment of the present invention, shown in FIG. 3. In FIG. 2A, a planar (e.g., thermal oxide) buffer layer 102 is shown formed over a silicon substrate 100. In FIG. 2b the planar waveguide core layer 104 (e.g., PSG) is shown formed over layer 102, which is then etched into the individual waveguide cores of FIG. 2C. Conventionally, this etching uses the underlying buffer layer 102 as an etch transition point (i.e., a material transition which can be detected during etching and therefore used to control the end point of the etch), but in accordance with one (optional) aspect of the present invention, this etching step continues into this buffer layer creating the "overetched" regions 105. This overetching has been shown to relieve some

waveguide stress, thus contributing to the stress engineered environment of the present invention. As discussed below, the stress field present in layer 102 results from, e.g., a CTE mismatch between layers 100 and 102. Overetching removes certain high stress points (near the lower corners of the cores) away from these cores. The depth of the overetch is preferably proportional to the stress in layer 106, e.g., the higher the stress, the higher the etch depth. For example, for a stress less than 10Mpa, an overetch of 1 μm or less may be adequate. For a stress greater than 10Mpa, an etch of greater than 1 μm, and up to or over 10 μm, can be used. (This overetch can also be used as a convenient etch transition point for SRG etch as discussed using FIGS. 6A-B below.)

[0030] FIG. 2D shows the overcladding layer 106 (e.g., BPSG) deposited over the cores (including into the overetched areas 105).

[0031] This overcladding layer 106 may be tailored for stress engineering, as follows: The primary stress in the system results from the CTE mismatch between the silicon layer 100 and the thermal oxide layer 102. For example, the CTE of layer 100 may be on the order of 3.5 parts per million (ppm), and that of layer 102: 0.7 ppm. The silicon layer 100 therefore contracts at about five times the rate of the thermal oxide layer 102. Though this stress is highest at this layer interface, the stress field extends to the upper surface of layer 102, to its interface with the cores (which themselves have a CTE of approximately 2.05 ppm).

[0032] Varying dopant levels can be used to tune the coefficient of thermal expansion (CTE) of the BPSG layer 106 according to that of the cores/undercladding/substrate. This doping is limited by the point at which the dopants diffuse out and negatively impact the index of refraction of this layer - known to be in the 8 mole percent range. To remove this stress field away from the cores, BPSG layer 106 is stress engineered by doping to, e.g., a CTE value of about 3.4 ppm (closer to that of silicon layer 100 - 3.5 ppm). By approximately matching the CTE of layer 106 to that of layer 100, a more symmetric stress field in layer 102 is obtained, and the center of that field is effectively moved away from its critical upper interface with the waveguide cores.

[0033] In accordance with the present invention, and with reference to FIG. 3, a passivation layer 108 is then deposited over BPSG layer 106, to create a chemical (e.g., vapor) barrier over the waveguides. In one embodiment, this passivation layer is specially tailored to avoid interference with the stress-engineered characteristics of the lower levels. This tailoring involves approximately matching the CTE of the passivation layer 108 to the CTE of the BPSG overcladding layer 106. "Approximately matching" as used herein connotes a CTE match to within about 10%. By using a particular composition, and carefully controlling the variables in the deposition process, this approximate match can be attained. A single passivation layer can be used, or multiple layers, if in their combination they remain compatible with the stress engineering techniques imposed in lower layers.

[0034] For example, a silicon nitride film can be used (e.g., Si_3N_4) with a thickness of .55μm optimized for stress of approximately -40+/-5Mpa. A plasma etched chemical vapor deposition (PECVD) process is used, with a deposition rate of approximately 1800 Å/min, 445 watts power @ 13.5 MHz, 555 watts @ 2.27 kHz, Ts=400 C, and pressure=3.3 torr. Exemplary deposition flows are: N_2=1600 sccm, SiH_4=500 sccm, NH_3=4000 sccm, with a resultant film refractive index of approximately 2.0350, and CTE of 3.4 ppm, i.e., approximately matched to that of BPSG layer 106. Passivation layer 108 therefore does not add any stress to the previously stress-engineered system over which it is deposited.

[0035] Any other suitable passivation materials may be used for layer 108, including for example, hydrogenated silicon nitride of the form $Si_xN_yH_z$; or silicon-oxy-nitride of the form $Si_xO_yN_z$ (with or without hydrogen).

[0036] FIGS. 4A-B depict another embodiment of the present invention. Layers 200, 202, 204 and 206 are formed in the same general way discussed above with respect to FIGS. 2A-D. Here, the stress engineering is effected primarily with stress release grooves (SRGs) 210 etched through the BPSG layer 206, between the waveguides. The SRGs can also be overetched into the undercladding layer 202, as in region 211. This overetching has also been shown to offer additional stress relief between adjacent

waveguides. SRG overetch can be used separately from, or in addition to, the stress engineering techniques discussed above like core overetch 105 (FIG. 2C) and BPSG layer doping.

[0037] In FIG. 4B, a passivation layer 208 is shown added to this structure - engineered to maximize the step coverage so that the walls and floor are covered. It is formed to not interfere with any stress engineering, by approximately matching its CTE to that of BPSG layer 206 as discussed above, and also by offering additional barrier protection along the sidewalls and floor of the SRGs (as a relatively thin layer so it does not interfere with the stress relief function of the SRGs).

[0038] FIGS. 5A-B depict yet another embodiment of the present invention. Layers 300, 302, 304 and 306 are formed in the same general way discussed above with respect to Figs. 2A-D. Again, the stress engineering is effected primarily with stress release grooves (SRGs) etched through the BPSG layer 306, between the waveguides. As in FIGS. 4A-B, this technique can be used separately from, or in addition to, the stress engineering techniques discussed above like core overetch 105 (FIG. 2C) and BPSG layer doping.

[0039] Here an additional buffer layer of undoped silicate glass (USG) 307 is added to the structure. This layer is formed on the upper planar surfaces of the structure, and along the SRG sidewalls and floor. When filling the SRGs, care must be taken to avoid complete fill by leaving a space or cavity 309 between the opposing vertical layers of USG. This cavity ensures the stress release function of the SRGs is maintained. This technique is useful when the core/SRG spacing is small enough to require additional optical buffer space, to avoid SRG interference with the optical performance of the cores.

[0040] For example, an undoped silicate glass (USG) can be used with a thickness of 1000 to 1500 Å optimized for stress of approximately -5 to -10 Mpa. A plasma enhanced chemical vapor deposition (PECVD) process is used, with a deposition rate of approximately 3448 Å /min, high frequency RF power of 700 watts, Ts=400 C, and pressure=2.6 torr. Exemplary deposition flows are: N_2=2050 sccm, SiH_4=260 sccm, N_2O=8000 sccm, with a resultant film refractive index of approximately 1.46 to 1.47, and

CTE of 3.4 ppm, i.e., approximately matched to that of BPSG layer 306. In this manner, USG layer 107 does not add any stress to the previously stress-engineered system over which it is deposited, and can therefore be relatively thick.

[0041] Passivation layer 308 can then be formed over this structure, as discussed above - here engineered to minimize the step coverage. The SRG cavities are controlled to be small enough, so that layer 308 remains generally planar, and only partially fills the cavities, as shown. Using this USG buffer advantageously ensures the integrity of the core optical characteristics; the integrity of the SRG stress release function; and further allows for a generally planar layer of passivation to be formed. This layer can also be relatively thick, if its CTE remains approximately matched to the PSG/BPSG layers immediately below.

[0042] Referring back to the passivated embodiments of FIGS. 3 and 5B, this passivation layer (108, 308) may be rather thin, on the order of .55μm. To prevent scratch damage to this barrier layer, it may also be desirable to add an additional layer of USG over this layer using the USG deposition techniques discussed above. USG is known to have more resistance to such physical impacts. Other suitable materials for this additional layer include for example, polyimide; benzocyclobutein (BCB) dielectrics; nitride-oxide-nitride sandwiches; or any polymer based coatings.

[0043] In all embodiments, the thicknesses can be, for example, USG: 1000 – 5000 Å, and silicon nitride: 3000–10000 Å.

[0044] FIGS. 6A-B depict yet another embodiment of the present invention. Layers 400, 402, 404 and 406 are formed in the same general way discussed above with respect to FIGS. 2A-D. Again, the stress engineering is effected primarily with stress release grooves (SRGs) 210 etched through the BPSG layer 306, between the waveguides. As in FIGS. 4A-B, this technique can be used separately from, or in addition to, the stress engineering techniques discussed above like core overetch 105 (FIG. 2C) and BPSG layer doping.

[0045] With reference to FIG. 6A, the core overetch proceeds down below the bottom surface of the cores by distance 413. This barrier between the filled BPSG layer 406 and undercladding 402 provides a detectable etch transition point boundary when etching SRGs 409. During SRG etch, this boundary can be detected, therefore providing a highly controllable SRG depth. This SRG depth control is much easier after over-etching the 6 μm cores, than when trying to accurately control the approximately 20 μm SRG etch depth.

[0046] As in FIGS. 5A-B, an additional buffer layer of undoped silicate glass (USG) 407 can be optionally added to the structure (FIG. 6B), and passivation layer 408 can then be formed over this structure, providing the same advantages discussed above.

[0047] Regardless of the particular selection of stress engineering features, the passivation layer is designed to be non-interfering (i.e., compatible) with their stress balancing properties, while providing all of the benefits of passivation, including its barrier to vapor, chemicals, etc. This barrier protection is becoming increasingly important as optical components are subjected to more adverse environments, and their related reliability standards and testing.

[0048] While the invention has been particularly shown and described with reference to preferred embodiment(s) thereof, it will be understood by those skilled in the art that various changes in form and details may be made therein without departing from the spirit and scope of the invention.